MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2017/2018

EEE4166 – DIGITAL INTEGRATED CIRCUIT

(All sections / Groups)

11 OCT 2017
9.00 a.m – 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This examination paper consists of 6 pages with 4 questions only.
2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Formulas:

Ideal diode equation: $I_D = I_S(e^{\frac{V_D}{\Phi T}} - 1)$

$$V_T = V_{TO} + \gamma(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|})$$

saturation:

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

linear:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

unified model:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DSAT} - \frac{{V_{DSAT}}^2}{2}\right)(1 + \lambda V_{DS})$$

$$t_P = \frac{C_L\frac{V_{SWING}}{2}}{I_{AVG}}$$

$$t_P = 0.69\,R_{eq}C_L$$

$$P_{dyn} = C_L{V_{DD}}^2 f$$

Question 1

(a) A simple diode circuit is shown in Figure Q1 (a).

(i) Assuming a silicon diode with $V_{D(on)} = 0.7$ V, determine current (I_D), voltage on R_1, R_2 and R_3 respectively. [6 marks]

(ii) If the voltage source V1 changed to 3 V, what is the new value for current (I_D)? [2 marks]

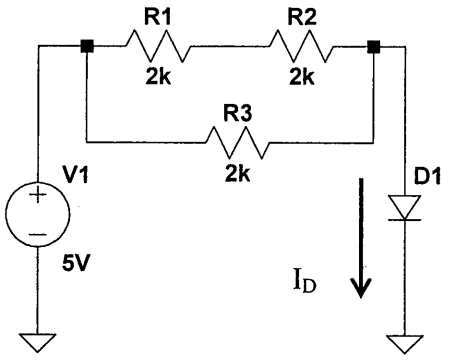

Figure Q1 (a)

(b) An NMOS transistor has aspect ratio W/L = 8/1 which is operating with $V_{SB} = 1.6$ V, $V_{GS} = 2$ V and $V_{DS} = 3$ V. Other parameter values for a minimum sized NMOS transistor are given as threshold voltage, $V_{T0} = 0.43$ V, $-2\varphi_F = 0.8$ V, body effect coefficient, $\gamma = 0.4\ \sqrt{V}$ and $k_n' = 115\ \mu A/V^2$. Determine the mode of operation and the drain current, I_D for this transistor. [6 marks]

(c) Calculate the diffusion capacitance (C_{diff}) for a transistor with given values: W = 1 μm, length $L_S = L_D = 2$ μm, and constants given as $C_j = 3.2 \times 10^{-4}$ F/m^2 and $C_{jsw} = 7.2 \times 10^{-10}$ F/m. [5 marks]

(d) An actual MOS device has deviated from its behavior of an ideal MOS transistor which gives several second-order effects. Explain the TWO secondary effects below:
(i) Hot carrier effect [3 marks]
(ii) Subthreshold conduction [3 marks]

Continued...

Question 2

(a) AVoltage Transfer Characteristics (VTC) graph is shown in Figure Q2.

(i) Redraw the VTC graph and label the critical voltages, V_{IL}, V_{IH}, V_{OL}, V_{OH} and V_M on the graph. [4 marks]

(ii) Derive the low noise margin, NM_L and high noise margin, NM_H using V_{IL}, V_{IH}, V_{OL} and V_{OH}.

[3 marks]

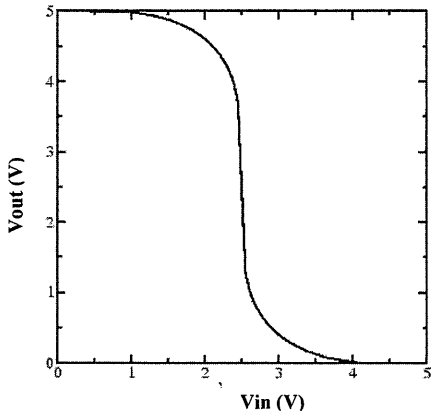

Figure Q2

(b) Given the function F below:

$$Y = AB + \overline{CD}$$

(i) Design a static CMOS gate realization of this function F with minimum transistor count. The input and inverted input ports are available for implementation.

[6 marks]

(ii) From the design in Part (i), compute the W/L ratios of the transistors so that the output resistance is the same as that of an inverter with $(W/L)_{NMOS} = 1$ and $(W/L)_{PMOS} = 3$.

[4 marks]

(c) In sequential logic, Schmitt Trigger is used to suppress noise.

(i) Describe the operation of the Schmitt Trigger, including its TWO important properties. [4 marks]

(ii) There are 3 types of astable multivibrators. Select TWO and explain its operations briefly.

[4 marks]

Continued...

Question 3

(a) A basic TTL NAND circuit is shown in Figure Q3(a). Assuming that the transistor has $V_{BE(on)} = 0.7V$, $V_{BE(sat)} = 0.8$ V and $V_{CE(sat)} = 0.1V$ with $V_{cc} = 5V$, $R_1 = Rc = 3$ kΩ.

(i) If either or both of the inputs to Q1 are in a low state (0.1 V), calculate the voltages v_{B1}, v_o and current, i_{B1}. [6 marks]

(ii) Modify or re-design the circuit in Figure Q3(a) to become Schottky TTL NAND gates. [4 marks]

(iii) Describe THREE advantages/features that Schottky TTL gates have, compared to the conventional TTL NAND gates. [3 marks]

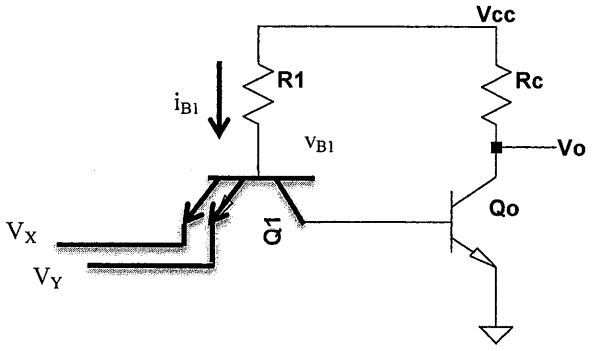

Figure Q3(a)

(b) Design a BJT inverter as shown in Figure Q3(b), to drive four identical inverters (N = 4) and to give $V_{OH} = 3.8$ V and $NM_L = 0.3$ V. The transistor has $I_{C(sat)} = 5$mA, $\beta = 100$, $V_{BE(cut\text{-}in)} = 0.6$ V and $V_{BE(sat)} = 0.8$ V. The supply voltage $V_{CC} = 5$ V.

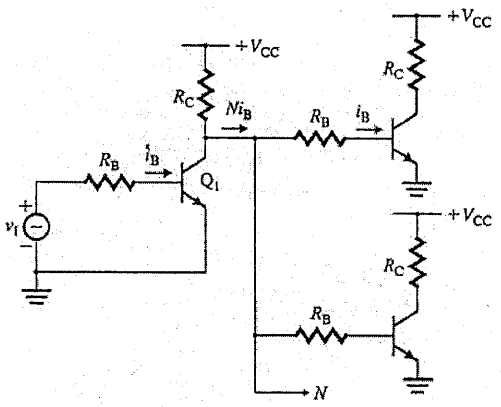

Figure Q3(b) [12 marks]

Continued...

Question 4

(a) Implement the following function using static CMOS gates:

$$F = A + B + \bar{C}$$

[8 marks]

(b) Given the load capacitance, C_L = 100 fF, voltage supply, V_{DD} = 3 V and clock frequency, f_{clk} = 250 MHz. Assume that the input signals are random. Based on circuit drawn in Part (a),

(i) Determine the dynamic power consumption, P_{dyn} of the circuit.
Hint: Use a truth table [6 marks]

(ii) Assume the leakage current is 3 nA and propagation delay is 2 ns, calculate the Power-Delay-Product (PDP) of the circuit.

[3 marks]

(c) Figure Q4 shows total power dissipation as a function of technology node.

(i) Based on this Figure Q4, comment on the proportion of the static power dissipation compared to dynamic power dissipation. [2 marks]

(ii) Critic and predict the total power dissipation for 32nm technology node.

[2 marks]

(iii)Recommend TWO methods to reduce the total power dissipation.

[4 marks]

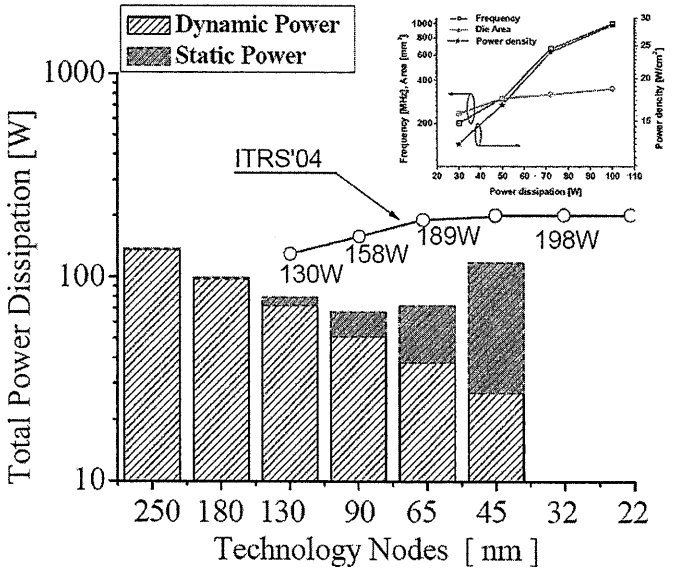

Figure Q4

End of Paper